Reference : H002-05-3.01-STD-B02	EN

User manual

PCIe-FIP

FIP / WorldFip Arbiter card

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1. OVERVIEW

1.1 GENERAL DESCRIPTION

This manual describes the PCIe Fip/WorldFip arbiter board. These communication boards are designed to fit into a PCIe slot and can be used in simple station mode, as well as, bus arbiter and station.

This board must be used with a dedicated software library for Linux environment.

The board can be declined for Fip datarates of 31.25kbps, 1Mbps or 2.5Mbps and with an optional termination impedance of 120 Ω or 150 Ω.

The PCIe bus responds to the *PCI Express Base Specification revision 2.0* and communicates with a 32 bits interface at 2.5 Gbps.

1.2 BOARD FEATURES

- WorldFip physical layer standard: IEC 1158-2;
- Fip physical layer standard: UTE C46-604;
- Medium redundancy management;
- Datarates available: 31.25kbps, 1Mbps and 2.5Mbps;
- Switchable termination impedances;
- Synchronization signal to trig different network;
- Status leds for state of the board and the channels;
- Size of 100 x 120 mm;
- Operating temperature: -40°C to +85°C.

2. BOARD ARCHITECTURE

2.1 FUNCTIONNAL ARCHITECTURE

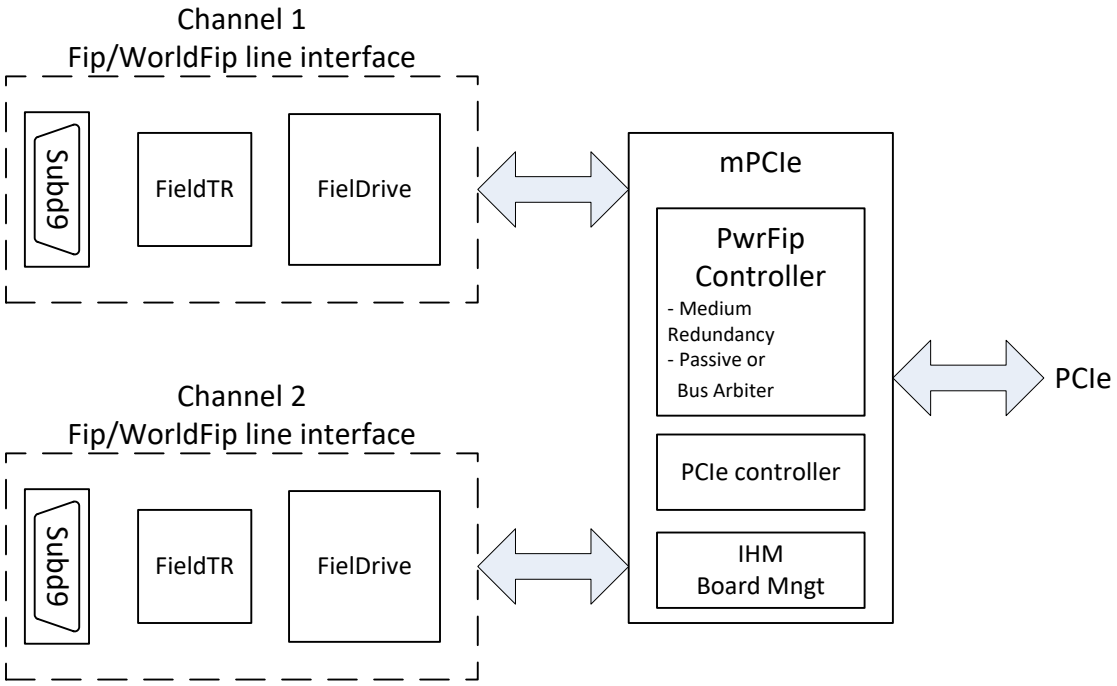


Figure 1: Functional block diagram.

2.2 PCIE INTERFACE

The PCIe interface is an integrated interface block inside the FPGA. It ensures compliance with the *PCI Express Base Specification revision 2.0*.

2.3 MPCIE

The mPCIe board integrates a fpga to allow transfers between host interface, memories, coprocessors and line interfaces.

2.4 COMMUNICATION COPROCESSOR

The communication coprocessor is a *PowerFip* component developed by Exoligent. This component implements the link and application protocols of the Fip and WorldFip fieldbus.
It integrates the medium redundancy to handle the both Fip/WorldFip channels.

2.5 LINE INTERFACE

Twisted pair lines are implemented using the *FielDrive* component and *FieldTR* transformers. Each interface exposes a Subd9 connector in conformance with the standard IEC 1158-2.

3. PHYSICAL CHARACTERISTICS

3.1 PHYSICAL DIMENSIONS

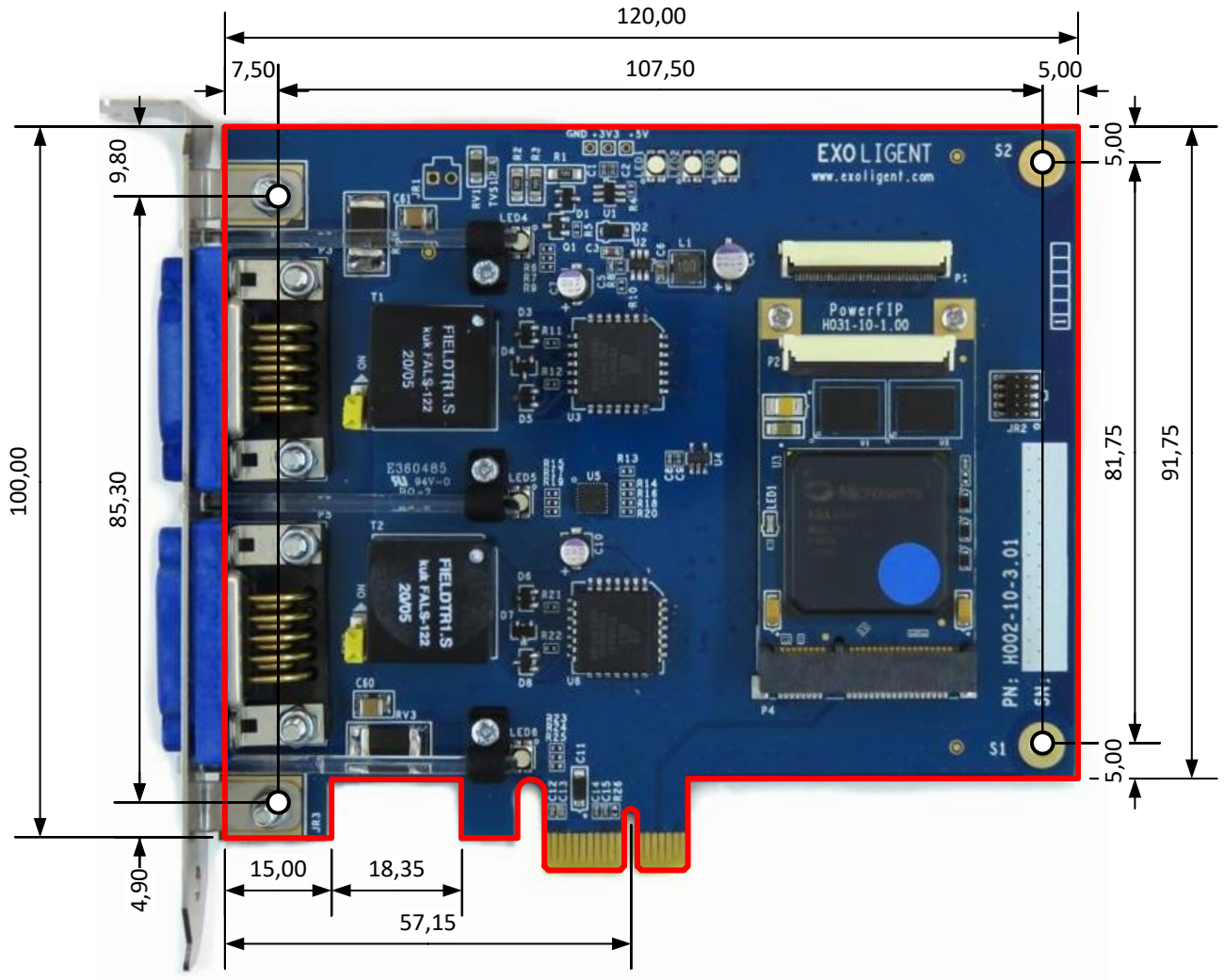


Figure 2: PCIe board dimensions.

3.2 FRONT PANEL

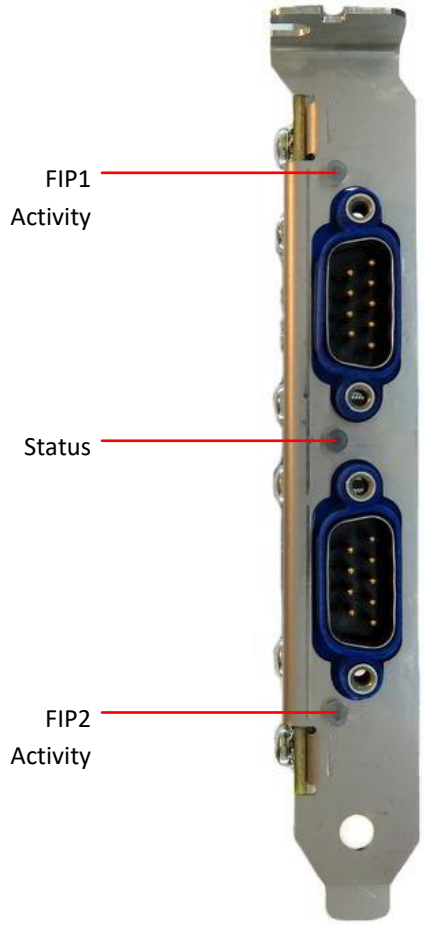


Figure 3: Front panel.

Status State of the board
• **GREEN :** Card ready. • **BLUE:** At power-up, blue or green blinks some times. And indicates traffic when communication is in progress by blink pattern. • **RED :** Fixed at startup and stay fixed => No PCIe initialization. Problem on the PCIe bus; Fixed red after starting software => An error occurs on the channel which was in use.
FIP 1 & 2 Activity State of the corresponding FIP line
• **BLUE:** Activity on the FIP line (Frames received). • **OFF**: Channel not used.

3.3 BOARD OVERVIEW

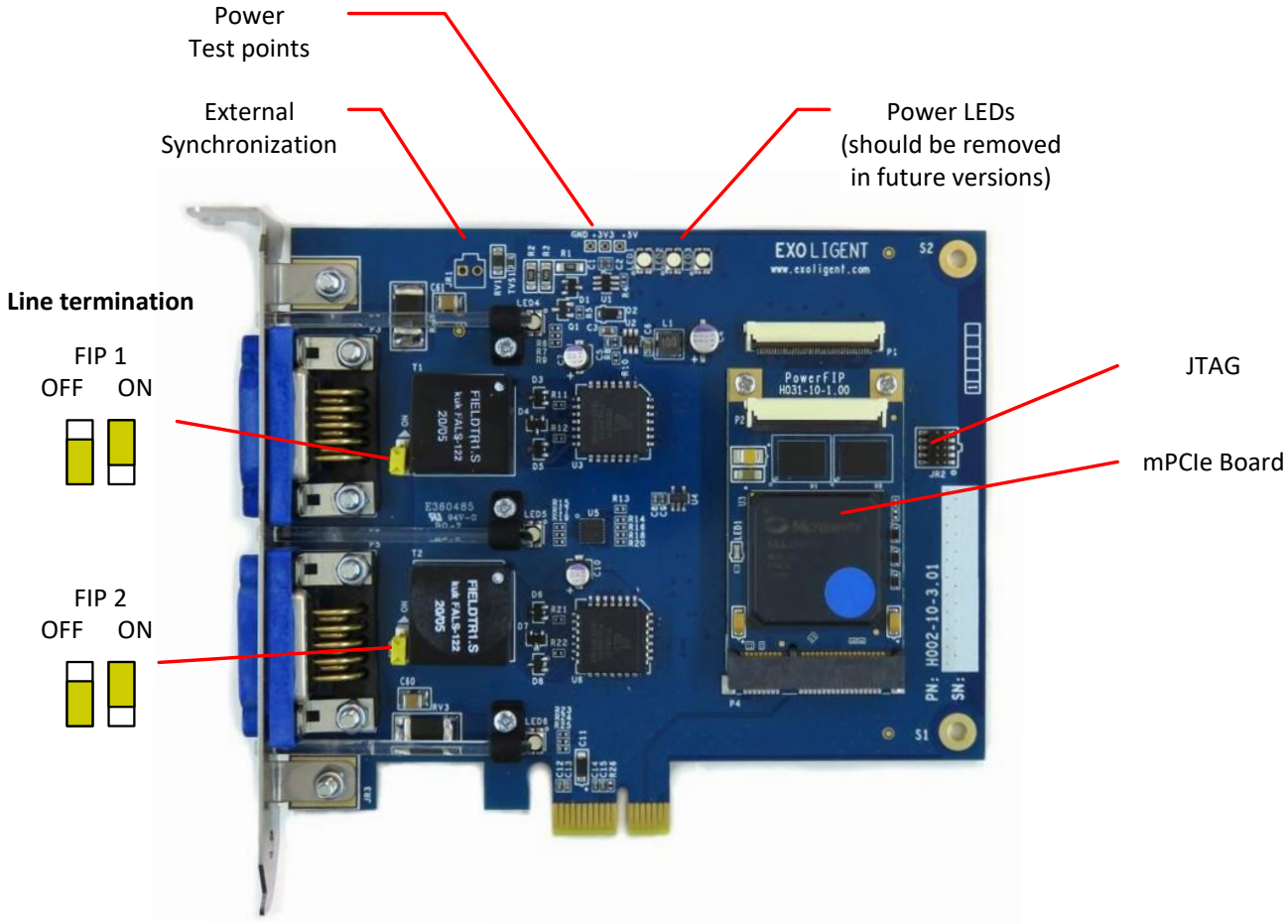
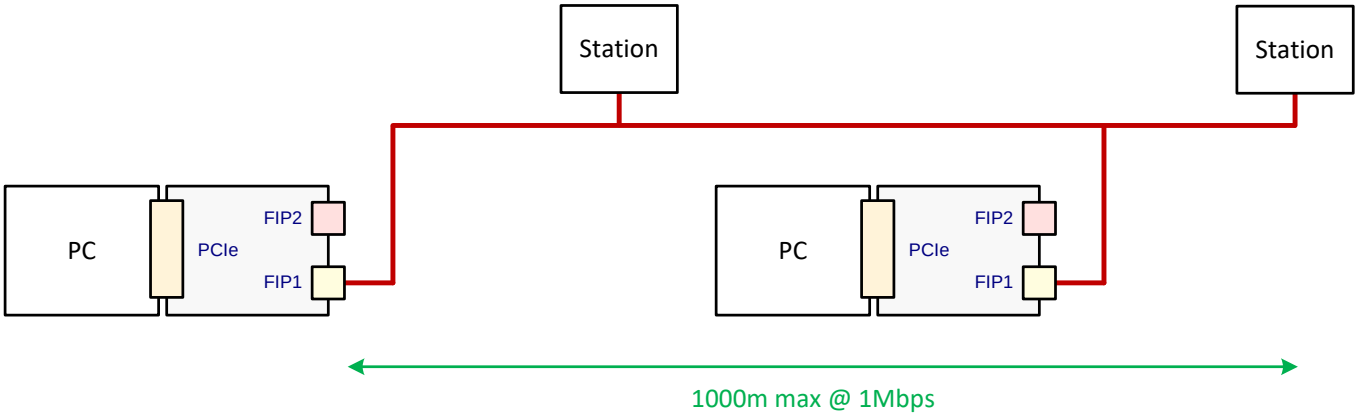


Figure 4: PCIe board overview.

4. TOPOLOGIES

4.1 SINGLE MEDIUM BUS TOPOLOGY

In this configuration, only one channel is used to communicate with other equipment.



4.2 DUAL MEDIUM BUS TOPOLOGY

In this configuration, two wired pair cables are connected in parallel on both channels to ensure redundancy and better security.